AMENDMENTS TO THE CLAIMS

This listing of Claims will replace all prior versions and listings of claims in the application:

LISTINGS OF CLAIMS

1. (currently amended): A non-volatile memory that comprises:

~~has~~ a ~~sequential access~~ SDRAM style memory interface, wherein said SDRAM style memory interface requires initialization prior to use;

SDRAM style address lines multiplexed in time, wherein a least significant portion and a most significant portion of an address are presented sequentially in two successive stages; and

SDRAM style sequential access logic incorporated in a logic subsystem, such that after a first address sequence is presented a second and subsequent address locations can be read using one or more additional SDRAM style control signals.

2. (original): A computer system that includes non-volatile memory and SDRAM, wherein the non-volatile memory shares a common interface with SDRAM.

3. (original): A method of initializing a computer system, comprising

reading boot code stored in a non-volatile memory, wherein the memory has a SDRAM style interface, and wherein the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface.

4. (original): A method of Claim 3, wherein subsequent memory locations are read by means of at least one control signal that functions independently of the SDRAM style interface and is received by sequential access logic incorporated in the non-volatile memory.

5. (original): A method of reducing control and address lines in a computer system having non-volatile memory and SDRAM, comprising

providing the non-volatile memory with a SDRAM style interface.

6. (original): A method of configuring a SDRAM interface in a computer system wherein the computer system has a non-volatile memory with a SDRAM style interface, comprising

storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory,

providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory, and

providing a least one control signal independent of the SDRAM style interface for incrementing the internal address of the non-volatile memory.

7. (original): A method of Claim 6, wherein the interface initialization code performs no branch operations.

8. (original): A method of Claim 6, further including storing system initialization code in the non-volatile memory, and including an instruction for copying at least a portion of the system

initialization code in the non-volatile memory into a random access memory, and a final instruction for branching to the system initialization code in the random access memory.

9. (original): A method of Claim 6, further including storing system initialization code in the non-volatile memory and including a jump instruction to a location in the non-volatile memory where at least a portion of the system initialization code is stored.

10. (original): A computer system comprising

non-volatile memory, and

volatile memory, wherein the non-volatile memory and volatile memory have a common interface.

11. (original): A computer system of Claim 10, wherein the interface is an SDRAM style interface which requires software-controlled initialization.

12. (original): A system of Claim 11, wherein interface initialization code for initializing the SDRAM style interface is stored starting at the first memory location in the first accessed memory row of the non-volatile memory.

13. (original): A system of Claim 12, further comprising at least one control line that is independent of the interface, for reading from the first memory location in the first accessed memory row, and at least one control line that is independent of the interface for incrementing the internal address register of the non-volatile memory.

14. (original): A system of Claim 12, wherein the interface initialization code for initializing the interface includes no branch operations until the system is ready to provide random access to memory.

15. (original): A system of Claim 12, wherein system boot code is stored in the non-volatile memory.

16. (original): A system of Claim 15, wherein a copy instruction is included after the interface initialization code, for copying boot code to a random access memory, and a branch instruction is included after the copy instruction for branching to the copied code in the random access memory.

17. (original): A system of Claim 15, wherein the interface initialization code is followed by a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored.

18. (original): A system of Claim 13, wherein the at least one control line for reading from the first memory location in the first accessed memory row, and the at least one control line for incrementing the internal address register of the non-volatile memory are one and the same at least one control line.

19. (original): A system of Claim 13, wherein different control lines are used for the at least one control line for reading from the first memory location in the first accessed memory

row, and the at least one control line for incrementing the internal address register of the non-volatile memory.

20. (original): A computer system comprising

a non-volatile memory having a SDRAM style interface.

21. (original) A system of Claim 20, wherein the non-volatile memory is Flash memory.

22. (original) A system of claim 21, wherein interface initialization code for initializing the SDRAM style interface is stored starting at the first location in the first accessed memory row of the non-volatile memory.

23. (original): A system of Claim 22, further comprising at least one control line that is independent of the interface, for reading from the first memory location in the first accessed memory row, and at least one control line that is independent of the interface for incrementing the internal address register of the non-volatile memory.